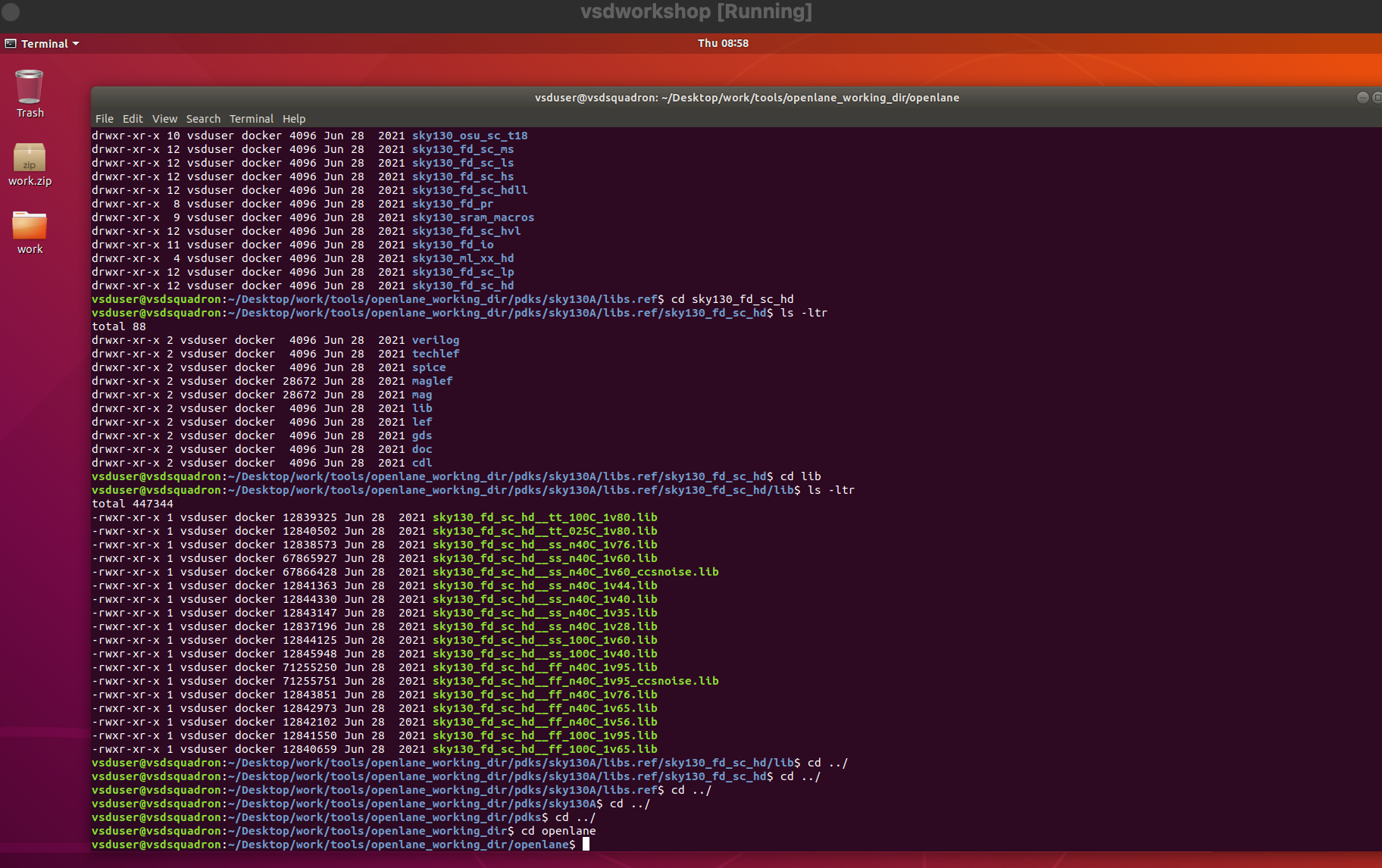
Day 1 was about how the chips enables us to create a way to talk to the computers.

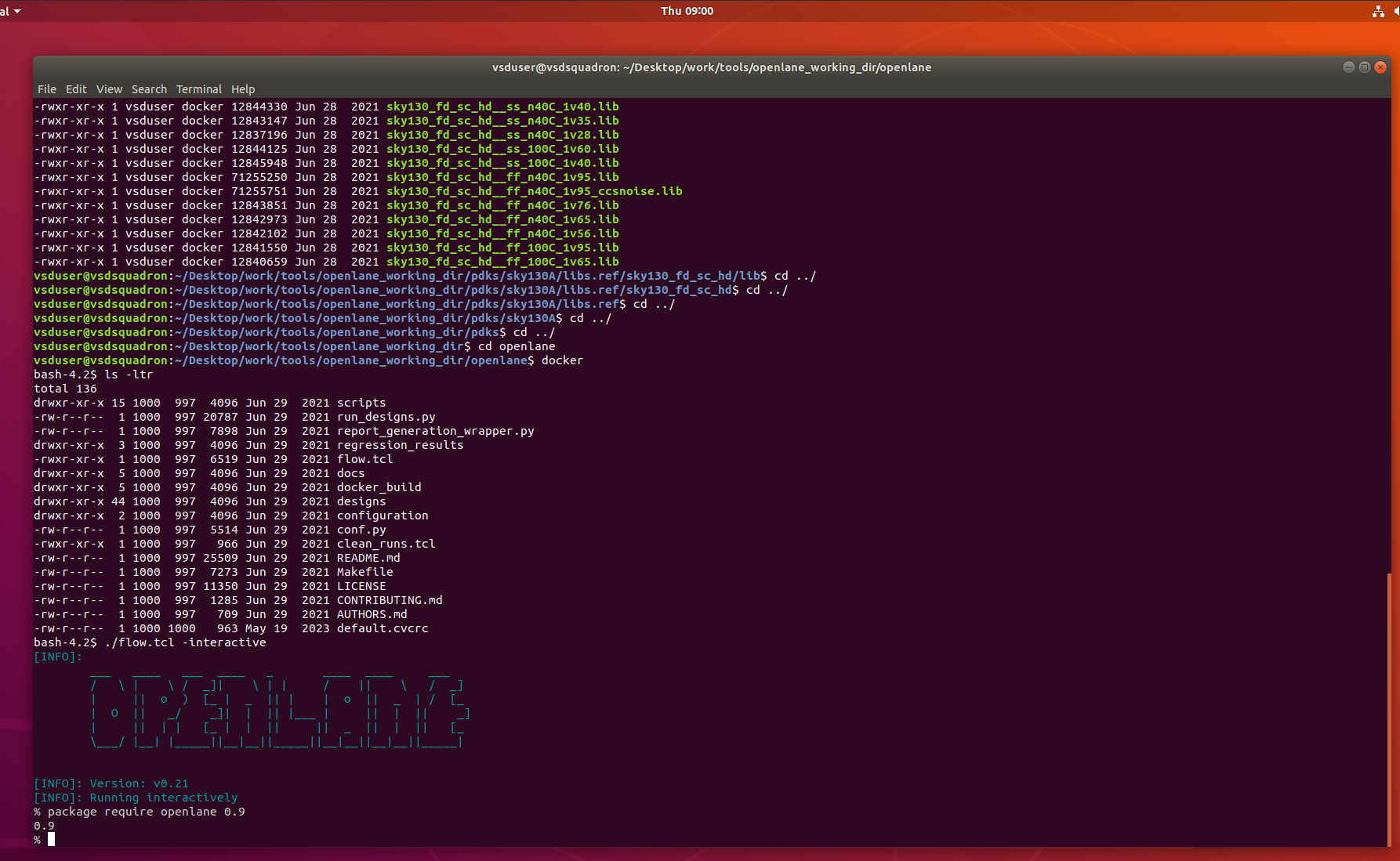
Instructor explained the basic purpose of this training, to match outputs from the test bench with the actual physical hardware via various iterations which will make sure the expected output is achieved.

Openlane platform explaination was given which is an automation platform that involves several tools like Yosys, Magic etch. This is an open source software so it can be used by academicians and industry alike. In summary the open lane checks for any conflicts in design rules or timing (even though at this project we may not strive to achieve best timing).

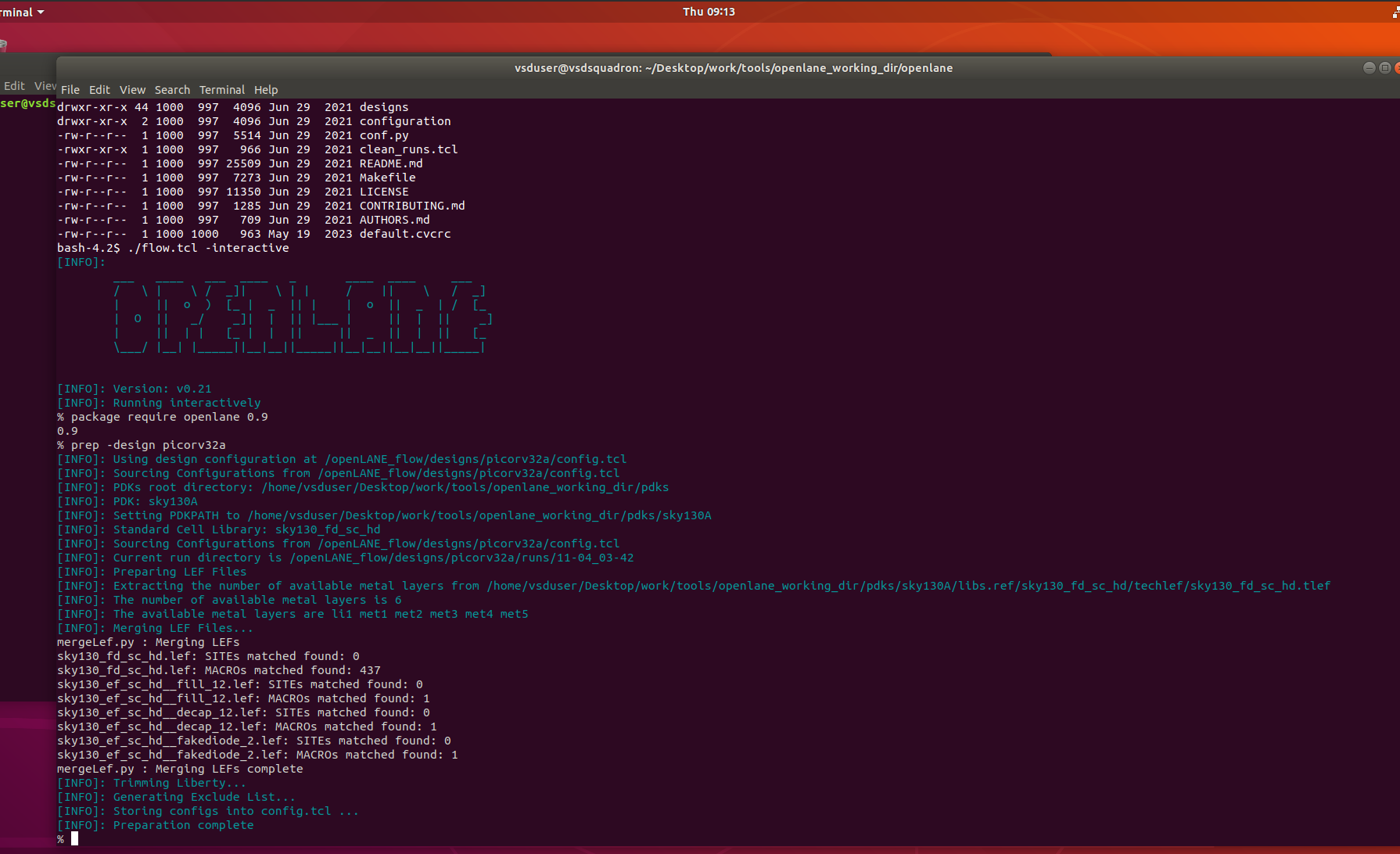
On the virtual box in desktop under work/tools folder the opelane software was located, we checked the sky130\_fd\_sc\_hb/lib and instructor explained content,



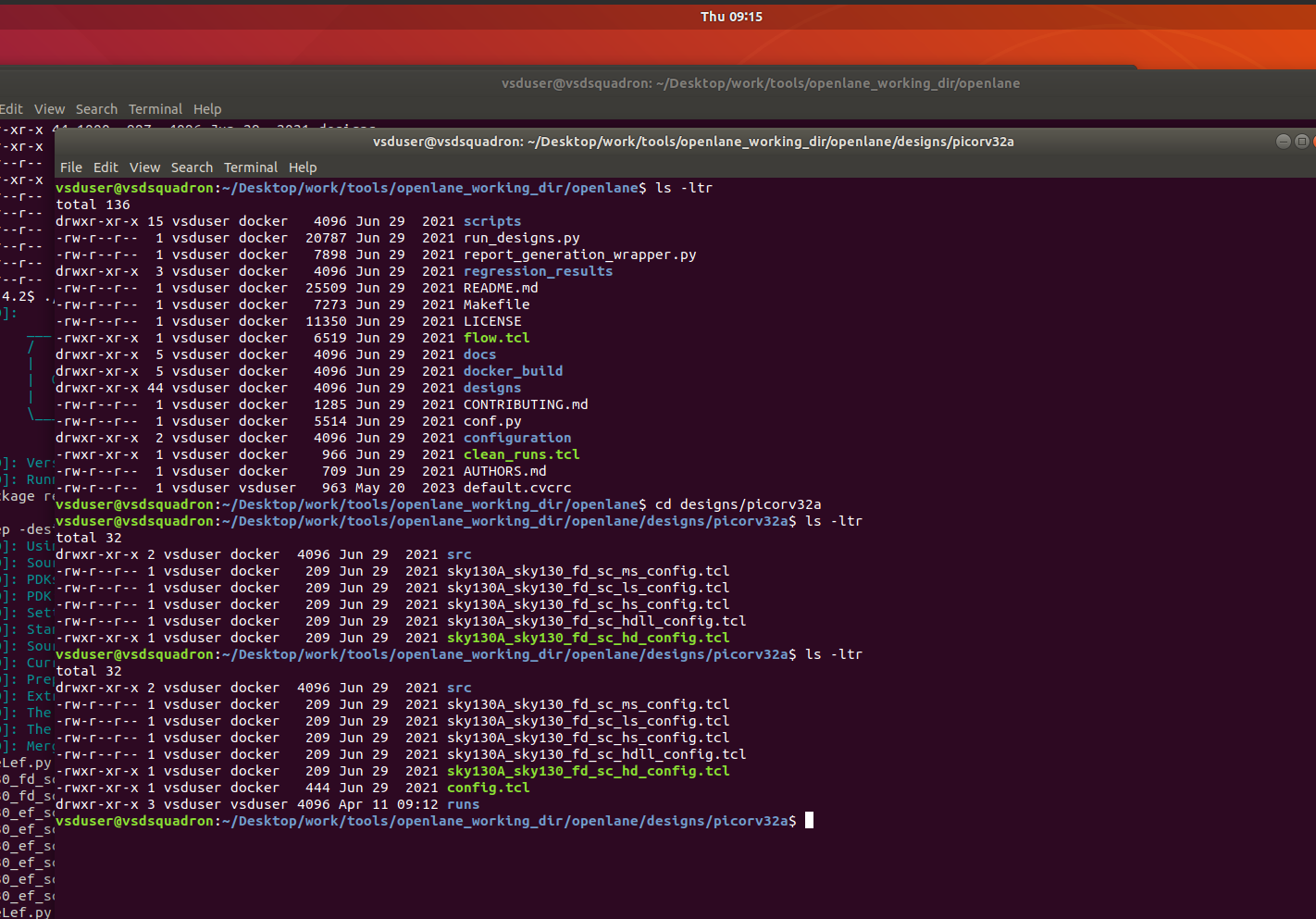
we opened that and executed the *docker* command and to view content we used the linux ls -ltr command, and we used *./flow.tcl -interactive command*



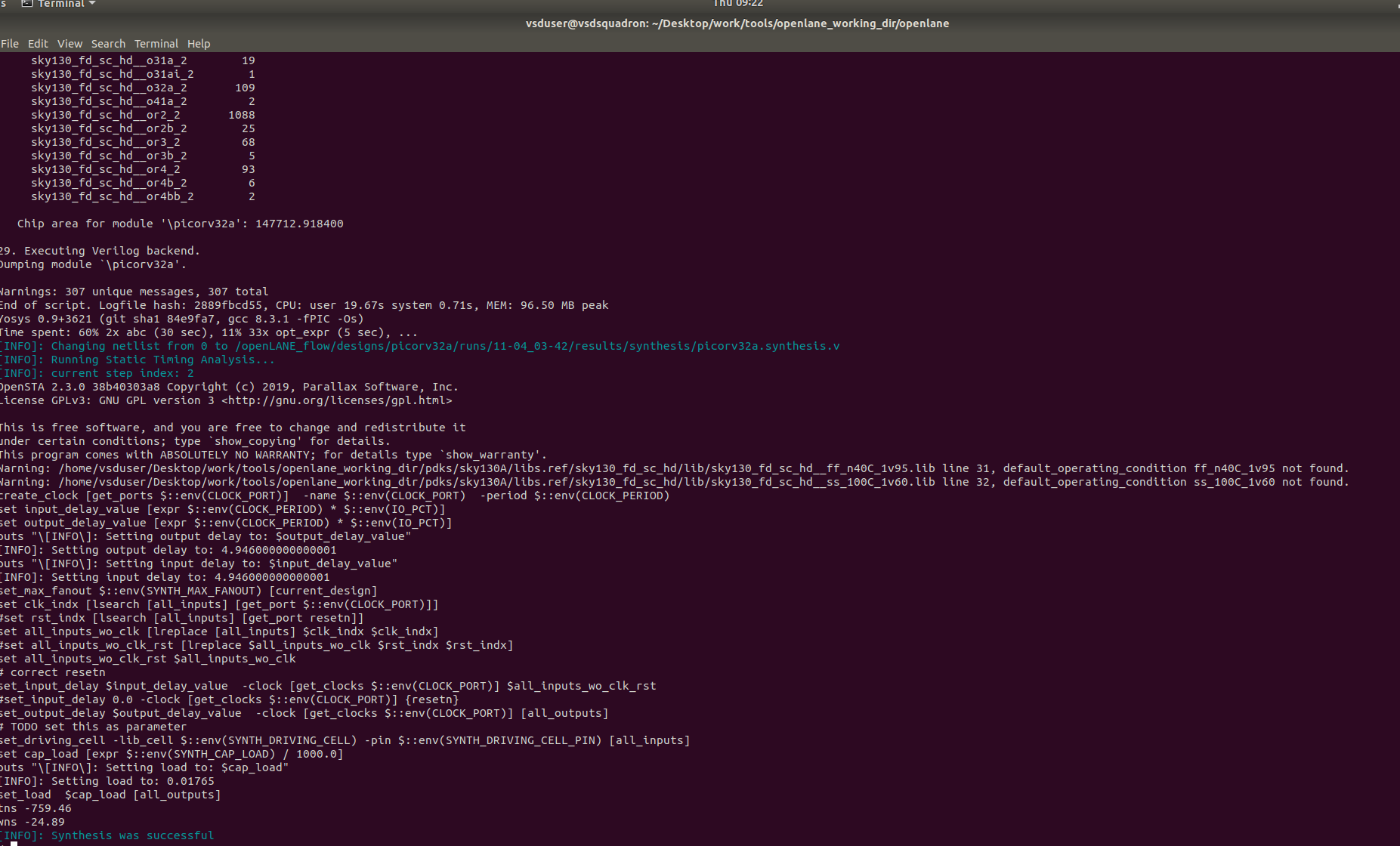
We are choosing picorv32a design and *prep -design picorv32a* command was used



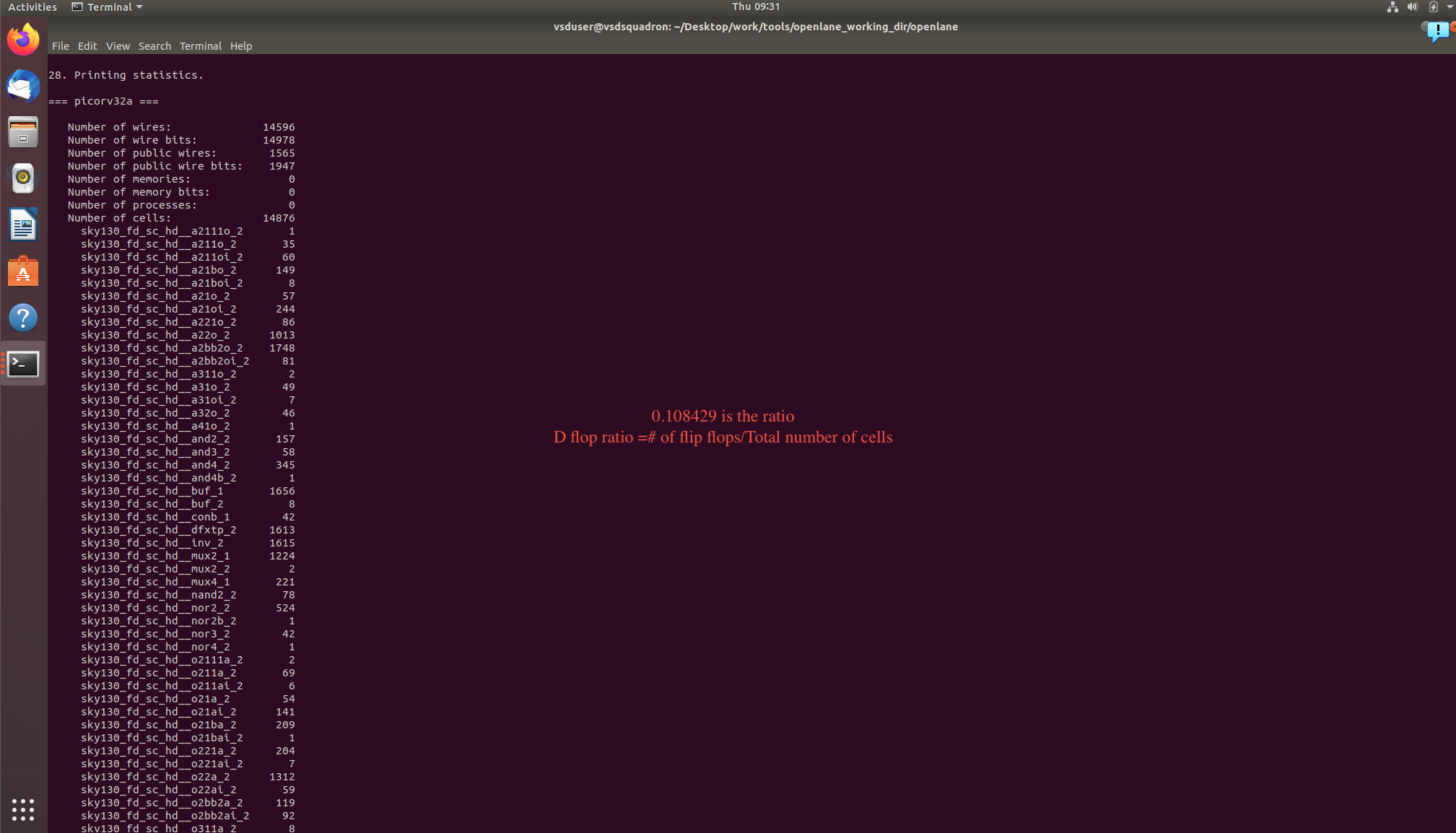
A folder for the executed date is created

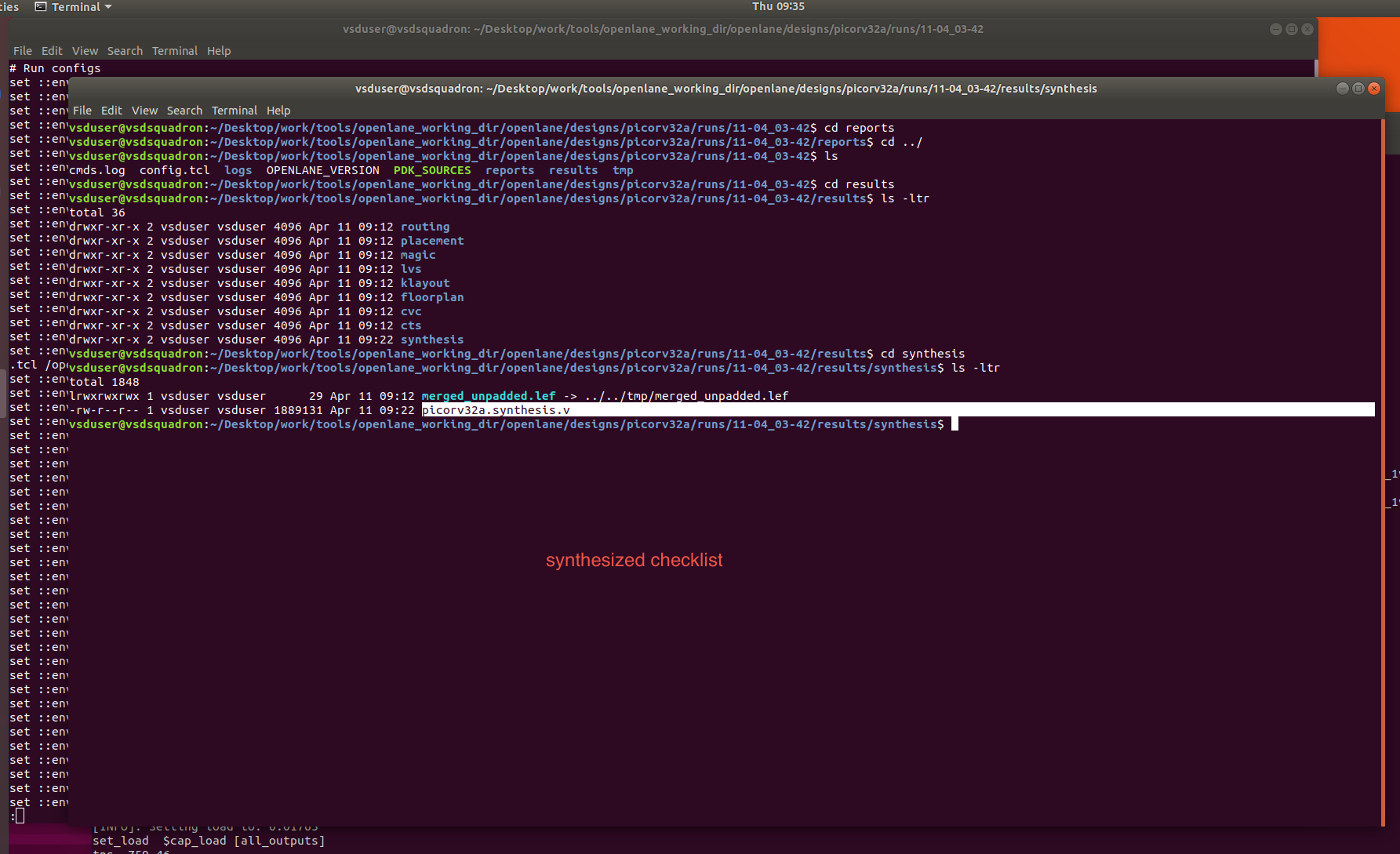


We use run\_sythesis command, it takes some time and upon completion of synthesis we can calculate the flop ratio which is the total flip flop divided by the total cells in design.



The flop ratio which I got was 10.8429%. After running the run\_synthesis command the result folder would have updated.





In reports we can confirm the ratio again.

